MIXED-SIGNAL DESIGN OF BIOPOTENTIAL FRONT-ENDS

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Abstract—High resolution Sigma-Delta Analog-to-Digital Converters (SDADC) have drastically changed traditional analog signal processing stages. However, as the boundary between analog and digital worlds becomes diffuse, a “mixed-signal processing” approach arises. For instance, analog filters, traditionally implemented as independent processing stages can be easily incorporated in the design of the Sigma-Delta converter, resulting in a more compact approach, with important advantages regarding size and power consumption. In this context, a design technique for mixed-signals front-ends intended for biomedical signals is presented here.

As an example, the design of an ECG front-end is presented. It accepts DC offsets of ±300mV, presents an AC input range of ±10mV, a -3 dB bandwidth of 100Hz and a total noise less than 10μVp-p, operating at a clock frequency of 57kHz. The front-end provides “fast baseline recovery” features and its transient response fulfills the AAMI standard. A functional prototype was built and tested, validating the design procedure.

Keywords—Biopotential Amplifier, AAMI Standard, Sigma Delta Converter, Mixed Signal Processing.

I. INTRODUCTION

Few decades ago, electrocardiograph recorders were entirely analog, from the electrodes to the graph printer. Nowadays, the tendency is toward fully digital equipment, leading to more flexible systems, which can be easily configured by software, without any hardware change. In order to achieve this, a direct analog-to-digital conversion is required, which implies null or minimum analog signal processing. Two approaches for this technique are shown in Fig.1. In the first one, depicted in Fig.1(a), the raw analog signal is converted to digital and all the operations, as gain adjust or dc removal, are made digitally, resulting in very flexible systems. This approach requires using ADCs with dynamic ranges of 20 bits or more to properly represent a small biopotential signal immersed in high DC electrode offset. Although general-purpose sigma delta ADCs with these resolutions are commercially available, a high clock frequency is needed in order to achieve the required resolution. This in turn increases power consumption, which is always a limited resource in battery powered circuits.

This work proposes a mixed-signal technique for biomedical front-ends that allows design of the SDADC transfer function, thus resulting in an efficient use of the available dynamic range. As an example, the design of an ECG front-end fulfilling the AAMI standard is also presented.

II. BASIS OF THE SIGMA DELTA CONVERTER

A simplified scheme of SDADC is shown in Fig. 2. It consists of a negative feedback loop that minimizes the difference between the integral of the input (vIN) and the integral of the digital output yD. So, the low frequency components of yD will correspond to vIN. The digital signal yD also contains quantization noise, which presents components up to one-half the sampling frequency.
Given that SDADC operates at sampling frequencies $f_{\text{CK}}$ much larger than the signal bandwidth $f_0$ (high oversampling ratios), quantization noise can be reduced by applying a digital low-pass filter, which reduces the noise bandwidth (Candy and Temes, 1992) and provides the SDADC digital output $d_{\text{OUT}}$. This signal, which corresponds to $v_{\text{IN}}$, has a residual quantization noise $n_0$.

The integrator in Fig. 2 can be implemented with switched-capacitor techniques or using a continuous time analog integrator. The proposed technique is intended for this later alternative.

The scheme in Fig. 2 (a) corresponds to a first order SDADC, but higher order SDADC can be designed increasing the number of integrators. The dynamic range of a SDADC, defined as the ratio between the rms value of the largest admissible sine wave and the rms noise $n_0$, is given approximately by (Candy and Temes, 1992):

$$ DR = \frac{\sqrt{2} (2L+1)}{\pi^L} \left( \frac{f_{\text{CK}}}{2 f_0} \right)^{L-1} $$

where $L$ is the order of the SDADC, $f_0$ the signal bandwidth and $f_{\text{CK}}$ the sampling frequency (clock frequency).

The $DR$ can also be expressed as a number of effective bits $NB$ given by (Pallàs-Areny and Webster, 1999):

$$ NB = \frac{20 \log 2}{\log f_{\text{CK}} f_0} $$

To improve the $DR$, the number of integrators $L$ and/or the oversampling ratio must be increased. The former implies greater circuit complexity, whereas the latter requires a higher clock frequency. Both of them increase power consumption. Expression (1) is valid for sinusoidal inputs. For other applications, like biomedical signals, $DR$ is usually estimated by simulation. In general, removing dc offsets, a dynamic range of 60-70dB ($\approx$10-12bits) is sufficient for biomedical applications.

Considering the SDADC transfer function between the continuous time input $v_{\text{IN}}$ and the digital output $d_{\text{OUT}}$, it can be analyzed as a continuous time transfer function $T_1(s)$ associated to the SD modulator, followed by a digital filter $T_2(z)$, as shown in Fig.2 (b).

### III. PROPOSED DESIGN TECHNIQUE

The proposed design technique implies distributing the required signal processing between the continuous transfer function $T_1(s)$ and the discrete transfer function $T_2(z)$.

$T_1(s)$ must be designed to reject high amplitude undesirable signals such as DC components, interference voltages or artifacts, in order to exploit ADC resolution on the signals of interest. This transfer function can be shaped increasing the order of the sigma delta converter (the number of integrators) and introducing feedback paths. The standard SDADC uses multiple feedbacks of the output ($\beta$ blocks in Fig. 3) allowing control only of pole locations and restricting $T_1(s)$ to implement low pass filters. Additional signal paths from the input ($\alpha_i$ blocks in Fig. 3) (Fergunon et al., 1990) allow assigning the zeros of $T_1(s)$, leading to the structure shown in Fig.3. It corresponds to the state-space canonical form named “second companion form” or “observable canonical form” (Friedland, 1986).

Assuming that the converter works properly, the comparator’s input is ideally null because it can be thought as an infinite gain block (Candy and Temes, 1992) and solving the scheme of Fig. 3 it results:

$$ T_1(s) = \frac{V_{\text{IN}}(s)}{V_{\text{OUT}}(s)} = \frac{\alpha_s s^{-1} + \frac{\alpha_s}{\prod_{i=1}^{L} \tau_i} + \frac{\alpha_i}{\prod_{i=1}^{L} \tau_i}}{\beta_s s^{-1} + \frac{\beta_s}{\prod_{i=1}^{L} \tau_i} + \frac{\beta_i}{\prod_{i=1}^{L} \tau_i}} $$

So, assigning appropriately the path gains $\beta_i$, $\alpha_i$ and the time constants $\tau_i$, it is possible to implement a target $T_1(s)$. Note that this transfer function is not sensible to $\tau_i$ because it precedes a comparator that is only sensible to the sign of its input.
Table I. Main AAMI electrocardiograph specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range of input signal ±5mV</td>
<td></td>
</tr>
<tr>
<td>DC offset voltage ±300mV</td>
<td></td>
</tr>
<tr>
<td>Upper cut-off frequency (3dB) 100Hz.</td>
<td></td>
</tr>
<tr>
<td>Allowable overshoot to step response (max)</td>
<td>10%</td>
</tr>
<tr>
<td>Decay time constant after step input (min)</td>
<td>3 sec.</td>
</tr>
<tr>
<td>System Noise RTI (max) 40μV p-p</td>
<td></td>
</tr>
<tr>
<td>Baseline return time after lead switch (max)</td>
<td>1 sec.</td>
</tr>
<tr>
<td>Baseline return time after reset (max)</td>
<td>3 sec.</td>
</tr>
</tbody>
</table>

$T_s(z)$ can be designed using standard digital processing techniques, regarding that it must be a low pass filter to reduce high frequency quantization noise. This noise decreases as the order (and the complexity) of the filter increases. In order to ensure a linear phase characteristic, general-purpose SDADCs use finite impulse response (FIR) filters. They require a large number of coefficients to achieve good high frequency attenuation. In custom problems, this filter can be designed specifically for the application and an infinite impulse response (IIR) filter with a reduced number of coefficients could be enough to fulfill particular requirements.

IV. TAILORING A SIGMA DELTA ADC TO THE AAMI STANDARD

As an application example, the design of an ECG front end fulfilling the AAMI standard is presented (AAMI, 1999). The main AAMI specifications are detailed in Table I.

In order to fulfill the required frequency and transient responses the following transfer functions were adopted:

$$T_1(s) = \frac{sτ_1}{1 + sτ_1}$$

$$T_2(z) = \frac{(1-a)^N}{(1-az^{-1})^N}$$

$T_1(s)$ provides DC rejection and a transient time constant $τ_1$ that must be greater than 3s. To implement a first order high pass filter ($n=2$), were adopted leading to the scheme of Fig. 4. In this case, SDADC transfer function is reduced to a high-pass filter as in Clancy et al. (2006) and Sadik et al. (2007).

To provide a fast baseline return from an overload saturation condition, a selectable constant was implemented (Fig. 5). A time constant $τ_1$ of 3.3 sec. was adopted in normal operation and $τ_1=70$ ms for a fast baseline return. This is controlled by the digital signal “FR” (Fast Recovery).

For $T_2(z)$, which provides bandwidth limitation, multiple real poles (see (5)) were adopted. This ensures a null overshoot fulfilling overshoot AAMI requirements (Spinelli et al., 2003) with a simple implementation. To obtain an attenuation of 3dB at 100Hz, coefficient $a$ must verify the following equation:

$$|T_1(f)| = \frac{1}{\sqrt{2}}$$

Given a desired noise level and signal bandwidth, in this case imposed by the AAMI standard, the order $N$ of the low-pass filter (5) and the over sampling ratio $0.5f_{ck}/f_0$ result from a trade-off between digital filter complexity and clock frequency. By simulation it was found that $N=8$ and an over sampling ratio of 256times easily fulfills noise specifications on Table 1 for a signal bandwidth of 100Hz, resulting $a=0.964$ and a clock frequency $f_{ck}$ of 57.6kHz (using available parts). Figure 6 shows the frequency response of the continuous transfer function $T_1(s)$ and the discrete transfer function $T_2(z)$.
V. PROTOTYPE IMPLEMENTATION

A functional prototype of the front-end was built and tested. \( T_1(s) \) was implemented by the single-ended (S-E) circuit shown in Fig. 5, where the flip-flop’s digital output levels were adopted as voltage references (compare with Fig. 2(b)). Powered at 5V, it has a DC input range close to \( \pm 2.5V \) and an AC range of \( \pm 0.50mV \). Including a difference amplifier with a gain of 5 times (Fig. 6), these ranges become respectively \( \pm 500mV \) and \( \pm 10mV \) referenced at the front-end input.

It is worth noting that the purpose of this circuit is only for validation of the proposed design technique. A practical circuit should have both differential input and output (Fully-Differential) and more precise voltage references should be used.

V. EXPERIMENTAL RESULTS

The experimental setup (Fig. 7) was completed with a microcontroller (ADUC841 of Analog Devices) that picks up the data stream provided by the front-end, packages and sends it by an optic fiber to a PC. Digital filtering \( T_2(z) \) was performed off-line on the PC side.

First, a 1mV peak-to-peak square wave was applied, resulting in the signal shown in Fig. 8(a), that verifies the required time constant of 3s. Then, using disposable electrodes E1, E2, E3 (see Fig. 7) real ECG data was acquired, resulting in the signal shown in Fig. 8(b). The front-end noise with the input short-circuited was less than 10\( \mu V \)p-p and the noise in the isopotential section of the ECG was less than 30\( \mu V \)p-p, which includes amplifier, SDADC, spurious signals and electrode noise. The AC input range was of \( \pm 10mV \) fulfilling the AAMI standard requirements.

![Fig. 7. Experimental setup used in the test of the \( \Sigma\Delta \) converter.](image)

![Fig. 8. Signals acquired with the implemented prototype. (a) Square wave response of the front-end and (b) acquiring real ECG data.](image)

Finally, to test the fast recovery (FR) feature, the circuit was intentionally saturated and the FR activated recovering baseline in less than 1 second. The low frequency distortion on the square wave in Fig. 9 clearly shows the segment where this mechanism was activated.

VI. CONCLUSIONS

A technique to design mixed signal biomedical front-ends, was presented. These circuits accept low level biopotential signals providing direct digital data and allow designing the analog-to-digital frequency transfer function. This later can be adapted for different biomedical applications.

Designing the SDADC specifically for the application, it is possible to make a better use of its dynamic range, leading to lower clock frequencies and thus reducing power consumption.

As an example, an ECG front-end according to the AAMI Standard was designed and experimentally tested. It provides direct digital data fulfilling the mentioned standard validating the proposed design procedure.

VII. ACKNOWLEDGMENTS

This work has been funded by the Universidad Nacional de La Plata through Project I127 and by Agencia Nacional de Promoción Científica (ANPCyT) through Project PICT 2007-005.

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