DISCRETE-TIME CONTROLLERS BASED ON THE INTERNAL MODEL PRINCIPLE FOR SHUNT ACTIVE POWER FILTERS

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***Abstract*— This paper presents an analysis and design of discrete-time controllers based on the internal model principle, applied to shunt active power filters. The presented control strategies are aimed to compensate the current harmonics produced by nonlinear loads connected to the point of common coupling in low voltage power grids. The proposed current controllers are based on the internal model principle operating with different sampling frequencies and for even and odd or only odd harmonics. It is demonstrated that the use of a downsampled rate, and fewer poles in the internal model, results in a straightforward digital implementation; improvement of the transient response; increasing of the stability margin of the closed-loop system and it is possible to obtain source currents with reduced total harmonic distortion. To validate the above claims and demonstrate the steady-state and transient performance, simulation results are presented.**

***Keywords*— Shunt active power filter, instantaneous power theory, internal model principle, downsampled controller.**

I. INTRODUCTION

The wide spread use of nonlinear loads such as uncontrolled rectifiers, electric motor drives, induction furnaces, electronic ballasts for discharge lamps and switching power supplies in a variety of power ranges; produces the injection of a high number of current harmonics in the low voltage power grids. This harmonics causes a distortion of the voltage waveforms in the point of common coupling with other loads. That distortion will be greater or smaller depending on the resulting impedance of the line section that being analyzed. In addition to, the current harmonics produce additional losses in the transmission lines and power distribution transformers, resonance effects with power factor corrector capacitors banks and malfunction of electronic equipment.

A classical solution to compensate the current harmonics is the use of shunt RLC notch filters. This results in a simple and highly efficient solution, but the good performance strongly depends on the equivalent impedance of the source. Additionally, the combination of this kind of filters with nonlinear loads and line impedance can cause undesired resonance effects resulting in high level voltage harmonics (Currence *et al.*, 1995). In the last years, by cost reduction and an improved of the power electronics reliability; there is a high preference to perform the compensation of current harmonics using shunt active power filters (SAPF). This results in an effective solution for low and medium power applications, reducing to acceptable limits the current harmonics injected by nonlinear loads (Bhattacharya *et al*., 1995; Akagi, 1996; El-Habrouk *et al*., 2000). Additionally, the SAPF in comparison to its passive counterpart allows a significant improvement of the transient response with load dynamic changes. Also, the control of SAPF can be done efficiently using digital control techniques programmed in DSCs (digital signal controllers) with reduced RAM. These devices allow a simple realization of control strategies which can only be done in the discrete-time domain; with the easily update of the different control techniques.

Concerning to the SAPF current control, exist an important contribution in the literature. The main used current control techniques are: hysteresis controllers, deadbeat controllers in stationary reference $\alpha\beta$ frame and synchronous reference dq frame, *plug-in* repetitive controllers in stationary and synchronous reference frames; and resonant controllers, also in both reference frames (Buso *et al*., 1998; Lindgren and Svensson, 1998; de Camargo and Pinheiro, 2005; Bojoi *et al*., 2005). The two last mentioned techniques, based on the internal model principle (Francis *et al.*, 1974) are implemented with considering that the sampling and switching frequency are the same. In the particular case of microcontrollers or DSCs with reduced RAM memory and low computational speed, the *plug-in* repetitive controller needs an important memory space with high sampling frequencies and require a high computational effort. Another drawback is that the system dynamic response is poor to load changes. This is due to the high number of delays of the periodic signal generator. Therefore, aiming to reduce the memory space, as well as the computational effort and even improve the overall performance of the system, in this paper it is demonstrated that an internal model based controller with a downsample rate allows achieving such improvements. This control strategy is named here *DSIM* or *downsampled internal model based controller*". Furthermore, the proposed internal model based controller strategies, depending on the structure of the periodic signal generator, makes it possible to compensate the even and odd current harmonics; or only odd harmonics. These proposals are validated with simulation results and a performance comparative analysis is carried out to highlights the improvements.

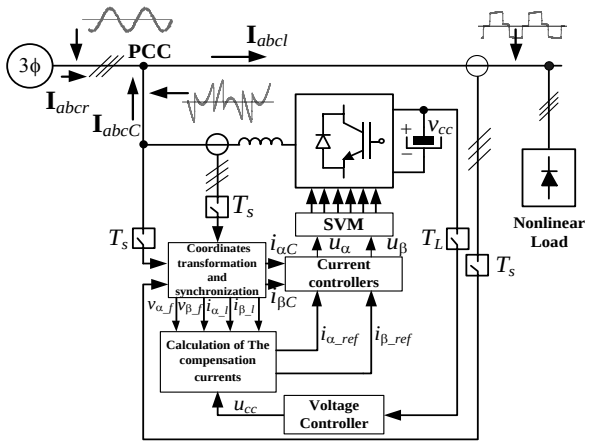

Figure 1: Control strategy of the SAPF.

Table 1: Electrical Specifications of the SAPF.

Nominal Power	15kVA
DC Link Voltage	500V
Input RMS Voltage	110V
Fundamental Frequency	50Hz
Switching Frequency, f_{sw}	10kHz
Sampling Frequency, f_s	5kHz or 10kHz
Base Voltage, V_{base}	500V
Base Current, I_{base}	21A

II. SYSTEM DESCRIPTION

A. Control Strategy

The proposed control strategy is presented in Fig. 1. The measured variables to control the system are transformed to be represented in two reference frames, the stationary $\alpha\beta$ and the synchronous dq. The references for the inner control loop are obtained in dq frame, due to the advantages for processing these signals in the synchronous frame. Since the internal model controller is implemented in stationary coordinates, then the above reference signals are transformed again to the $\alpha\beta$ frame. This implementation reduces the complexity of the control algorithm, since the system is decoupled, obtaining independent current controllers for each axis.

For the DC link voltage regulation, this outer loop is designed with the same model as described in Dose *et al*. (2010), with a sampling frequency equal to the double of the grid voltage fundamental frequency. The three-phase voltage source converter is modulated by SVMPWM, with a symmetric switching sequence (Pinheiro *et al*., 2005), reducing the THD of the converter synthesized voltages. The SAPF parameters are presented in Table 1**.**

B. Synchronization Algorithm

For the different realizations of the internal model based controllers, the synchronization of the converter with the grid voltages were carried out using the *NPSF* algorithm, which takes into account the imbalance and distortion of the grid voltages (De Camargo and Pineiro 2006). The block diagram that resumes the *NPSF* synchronization algorithm is shown in Fig. 2. The synchronization signals, cos(θ) and sin(θ), are obtained in the following form:

$$\sin(\theta)=\frac{v_\alpha}{\sqrt{v_\alpha^2+v_\beta^2}},\quad \sin(\theta)=\frac{v_\beta}{\sqrt{v_\alpha^2+v_\beta^2}}. \tag{1}$$

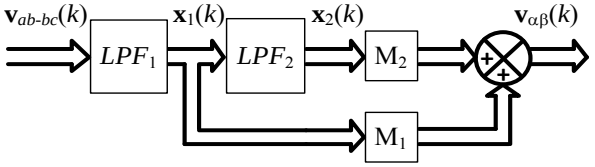

Figure 2: NPSF algorithm block diagram.

The low pass filters LPF_1 and LPF_2 shown in Fig. 2 are implemented with a 16 bit word length, obtaining in this way synchronization signals with a reasonably low harmonic distortion. M_1 and M_2 are matrices that transform the line-to-line voltages to fundamental positive sequence phase voltages in $\alpha\beta$ frame, and are given by:

$$\mathrm{M}_1=\frac{1}{2}\begin{bmatrix}0 & -\sqrt{2}/2\\ \sqrt{6}/3 & \sqrt{6}/6\end{bmatrix},\quad \mathrm{M}_2=\frac{1}{2}\begin{bmatrix}-\sqrt{6}/3 & -\sqrt{6}/6\\ 0 & -\sqrt{2}/2\end{bmatrix}. \tag{2}$$

III. REFERENCE SIGNAL GENERATION FOR THE COMPENSATION CURRENTS

Since the particular interest of the SAPF is to compensate the load harmonics currents in order to obtain sinusoidal and balanced currents from the source at the PCC (i.e., $\mathbf{I}_{abcr}$ in Fig. 1), based on the instantaneous power theory (Akagi *et al*., 1999), the computation of the compensation currents requires only the fundamental and positive sequence components of the sources voltages. The compensation powers in an arbitrary reference frame are computing with the following equations:

$$p=v_x i_x+v_y i_y,\quad q=v_x i_y+v_y i_x. \tag{3}$$

Using the synchronous reference dq frame, the fundamental and positive sequence components of the grid voltages in this reference frame, can be determined by the following expressions:

$$v_{d\_f}^{+}=V_p\sqrt{3/2},\quad v_{q\_f}^{+}=0. \tag{4}$$

where V_p is the peak value of the fundamental positive sequence component of the source voltages. Substituting (4) in (3) the resulting compensation powers are shows in Eq. (5).

$$p=i_{d\_c}V_p\sqrt{3/2},\quad q=i_{q\_c}V_p\sqrt{3/2}. \tag{5}$$

where i_{d_c} and i_{q_c} are the load currents in dq frame. To perform the compensation the SAPF must inject at the PCC, the reactive component equals to i_{q_c} and the harmonics from i_{d_c}. To obtain the harmonics of i_{d_c}, it is necessary to extract the DC component from this signal; that is equivalent to extract the fundamental component from the harmonics in the stationary reference *abc* frame (Botterón and Pinheiro, 2005). For this purpose, a second order high pass filter (HPF) is designed to eliminate only the DC component from i_{d_c}. The resulting filter presents a negligible phase delay to the rest of the signal components. The sampled transfer function of HPF is given by:

$$G_{HPF}(z)=\frac{z^2-2z+0.9995}{z^2-1.956z+0.957}. \tag{6}$$

The frequency response of this filter is given in Fig. 3.

Once the reference signals for the inner control loop in the reference *dq* frame are obtained, they must be transformed to the stationary reference $\alpha\beta$ frame to finally compute the current controllers.

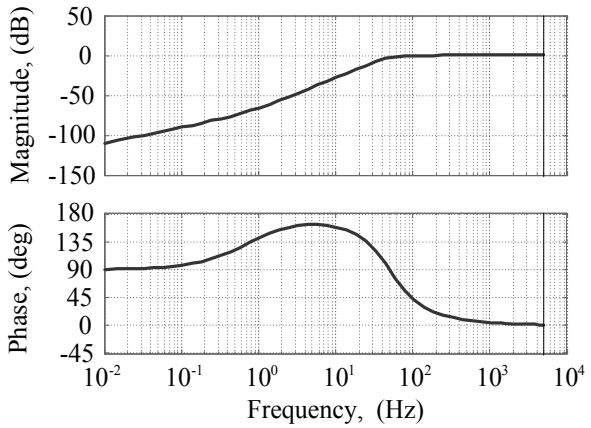

Figure 3: High pass filter frequency response implemented to separate the DC component form i_{d_c}.

IV. SYSTEM MODEL IN THE STATIONARY REFERENCE $\alpha\beta$ FRAME

The controller of the SAPF currents is developed in $\alpha\beta$ frame which results in two SISO plants, being possible to design in a separated form, two decoupled controllers. Because to the digital implementation of these controllers is necessary to consider the delay introduced by the A/D conversion of the variables of interest and the time calculation of control actions. In this case, to model this delay is considered an entire sampling period. Finally, the discrete-time model of the plant, for any of the axis, is:

$$G_p(z) = -\frac{T_s}{L}\frac{V_{base}}{I_{base}}\frac{1}{(z-1)z}, \qquad (7)$$

where T_s is the sampling period, L the inductance of the plant, V_{base} and I_{base} are the voltage and current base values used to normalize the discrete-time model. These base values simplify the digital realization of the control strategy in the DSC, and limit the dynamic range of the variables of interest according to the selected fixed point format. V_{base} and I_{base} are relating to the DC link voltage and the nominal per-phase peak value of the current respectively.

V. THE INTERNAL MODEL BASED CONTROLLER

To achieve an asymptotic tracking of the reference compensation currents, the implementation of the discrete-time controllers based on the internal model principle that use periodic signal generators (Botterón and Pinheiro, 2007), is an attractive solution because of its simplicity of digital realization. This structure does not present rounding problems and its digital realization results in a simple difference equation, with a reduced computational effort; in comparison to other compensators structures based on the same principle (Rodriguez *et al*., 2009; De Heredia *et al*., 2006; Lascu *et al*., 2007).

A. Even and odd harmonics compensators

The general compensator structure uses the periodic signal generator in parallel with a proportional compensator (Botterón and Pinheiro, 2007), as shown in Fig. 4, where $G_{mi}(z)$ has the desired dynamics to track, and $G_c(z)$ is a classical compensator used to stabilize the closed-loop system and improve the dynamic response.

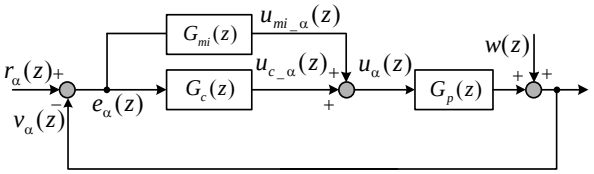

Figure 4: Block diagram of the control strategy that uses an internal model based controller in parallel with a classical compensator.

Figure 4 represents the control scheme for the α-axis. A similar scheme must be draw for the β-axis. Hereinafter, the equations written for the α-axis controller are used also for the β-axis.

The transfer function of the internal model based controller, $G_{mi}(z)$ is given by:

$$G_{mi}(z) = -\frac{k_{mi}z^d}{z^N - 1}. \qquad (8)$$

In the Eq. (8), N is the number of poles placed on the unit circle in the z-plane and represents the number of harmonics to track (or compensate). Note that this controller can compensate only the harmonic frequencies until the Nyquist frequency, that is, $f_s/2$. N is calculated by the quotient between the sampling frequency and the fundamental frequency of the grid voltage. The parameter d is a number of discrete advances that compensate the phase delay introduced by the internal model poles in the closed-loop system and improve the relative stability at high frequencies (Botterón and Pinheiro, 2007). Finally, k_{mi} is the internal model controller gain, which has an influence on the tracking error and the transient response of the system.

In the control scheme of Fig. 4, both the internal model controller and the classical compensator are sampled (or computed) to the same frequency. If the sampling frequency is higher, the parameter N increases as well, introducing a higher number of delays in the controller structure, which requires a significant memory space to implement the controller. In addition, the system performance is depreciated, presenting a poor transient response. Based on the aforementioned, it is possible to reduce the poles of the internal model reducing the sampling frequency of the internal model based controller, reducing as well, the number of harmonics to compensate. This strategy requires less memory space, improves significantly the system performance during transients, and also increases the relative stability of the closed-loop system (Botterón and Pinheiro, 2007).

B. *DSIM* controller: Even and Odd harmonics

Based on the exposed above, next the *DSIM* (*downsampled internal model*) controller is presented (Botterón and Pinheiro, 2007); in which the control ac-

tion of the internal model based controller is computed at half (or a quarter) of the computation rate of the classical compensator. The discrete time system with this kind of controller is shown Fig. 5 and the transfer function of the *DSIM* based controller is given by (9).

$$G_{mi}(z_{mi}) = -\frac{k_{mi} z_{mi}^{d}}{z_{mi}^{N} - 1}. \quad (9)$$

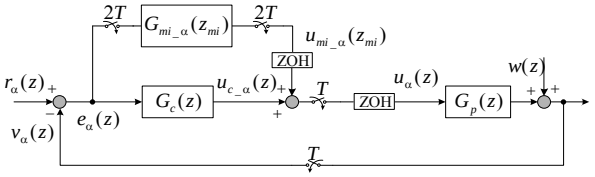

Figure 5: Block diagram of the *DSIM* control strategy.

where, $z_{mi}=e^{T_{mi}s}$ and $T_m=2T_s$ (or $4T_s$), being T_s the sampling period of the classical compensator.

Note that *DSIM* structure, reduces to a half (or a quarter) the size of the buffer (memory space) required to digitally implement the proposed controller strategy. Also, the reduction of *N* results in a better transient response of the overall closed-loop system.

C. Odd harmonics compensator

Considering that the typical nonlinear loads connected to three phase systems (i.e., three phase or single phase uncontrolled rectifiers, with or without capacitive filter) drain nonlinear currents whose waveforms have odd harmonics, the utilization of the periodic signal generator for odd harmonics proposed in (Griñó and Castelló, 2004), offers good results for this application. The transfer function of the resulting odd harmonics internal model based controller it is given by:

$$G_{mi}(z) = -\frac{k_{mi} z^{d}}{z^{N/2} + 1}. \quad (10)$$

This odd harmonic controller, computed at the same frequency of the classical compensator, has similar characteristics of the previous *DSIM*, achieved a good transient response and increasing the relative stability of the closed-loop system. Note that to digitally implement this controller, the internal model of (10) require a buffer size equal to the half of the buffer size used in the internal model based controller given by (8). The only limitation is that this controller only can compensate odd harmonics. In addition, a further improvement can be achieved with a downsampled or *DSIM* odd harmonics internal model based controller. In this case the transfer function given by (11) is sampled at the half of the sampling frequency of the classical compensator, further reducing the buffer size which is now the half of used in equation (10). The transfer function of the resulting *DSIM* odd harmonics internal model based controller it is given by:

$$G_{mi}(z_{mi}) = -\frac{k_{mi} z_{mi}^{d}}{z_{mi}^{N/2} + 1}. \quad (11)$$

D. Difference Equations for the DSC implementation

The difference equations to implement the previously described controllers are obtained applying the $\mathcal{Z}$ transform to the Eq. (8), (9), (10) and (11). The difference equation for the α-axis (idem for the β-axis) result as shown in Eq. (12).

$$u_{mi\_\alpha}(k) = k_{mi} e_\alpha(k - N + d) + u_{mi\_\alpha}(k - N). \quad (12)$$

In the last difference equation, the parameters *N* and *d* may vary depending on the used control strategy and also, in the case of the odd harmonics internal model based controllers, the second term of (12) becomes negative. On the other hand, the classical compensator to stabilize the control systems, used in the proposed control strategies, is a proportional gain, and the control action $u_{c\_\alpha}(k)$ is given by:

$$u_{c\_\alpha}(k) = k_p e_\alpha(k). \quad (13)$$

VI. CONTROLLER DESIGN AND STABILITY ANALYSIS

The parameters k_{mi} and *d* in transfer functions (8), (9) and (10), and also the gain K_p of the proportional compensator, defines the global stability of the closed-loop system. The proposed methodology to establish these values for the cases described in Section 5 and specifically in subsections A and B, is described below:

1) Insertion of the transfer function $G_{mi}(z)$ in tandem with the plant, starting with a small gain k_{mi} (0.05) to not affect the stability of the closed-loop system, the *d* parameter is found by trying different values starting from one, increasing it until the closed-loop poles are introduced inside the unit circle, with the exception of the poles near to z=1, that is, the dynamic of the plant. These poles are stabilized by adding the proportional compensator K_p.

2) The next step is to introduce the proportional gain K_p, to gain stability and improve dynamic performance. The value of K_p is chosen based on performance specifications.

3) Finally, the gain k_{mi} is increased until obtain an acceptable transient response of the tracking error signal.

Figure 6a illustrates the location of the closed-loop poles when the internal model based controller with d=2 is introduced. It is possible to observe that the red points indicate the unstable poles near to z=1. Figure 6b presents the pole-cero constellation when both controllers are included in the closed-loop system. It is possible to see that the global stability is accomplished with adding the classical compensator.

In case of *DSIM* controllers, the compensator parameters are establishes in the same manner. However, to analyze the stability of the closed loop system, is required to find the equivalent discrete-time model of the plant in series with the classical compensator, at the same sampling frequency of the internal model based controller and to analyze the closed-loop poles of this equivalent transfer function in tandem with $G_{mi}(z_{mi})$ (Botterón and Pinheiro, 2007).

In this work there is an additional proposal, which is the reduction of the sampling frequency of the classical compensator at half of the switching frequency. This allows decreasing even more the buffer size needed for *DSIM* strategies, significantly improving the SAPF

steady-state and transient performance. Regarding the design procedure of the compensator parameters, the methodology is exactly the same as above described for the cases where $f_s = f_{sw}$.

The set of the controller parameters for the six cases proposed in this paper, are presented in Tables 2 and 3. In all cases, the parameter d=2.

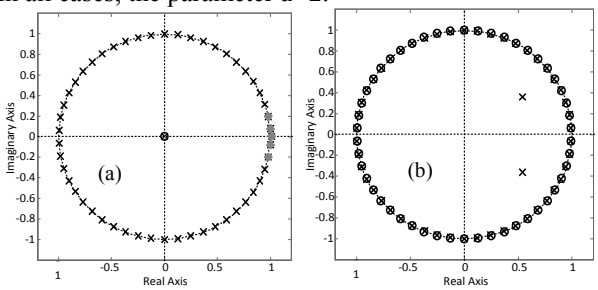

Figure 6: Pole-zero constellation of the system with (a) $G_{mi}(z)$ in tandem with the plant, d=2, and f_s = 5kHz. (b) Both controllers in closed-loop.

Table 2. Controller parameters for $f_s = f_{sw}$

Internal Model Controllers	N	K_p	k_{mi}
Even and odd harmonics	200	-0.5	0.05
Odd harmonics	100	-0.5	-0.05
Even and odd harmonics *DSIM*	100	-0.5	-0.2
Odd harmonics *DSIM*	50	-0.5	-0.2

Table 3. Controller parameters for $f_s = 0.5f_{sw}$

Internal Model Controllers	N	K_p	k_{mi}
Even and odd harmonics DSIM	50	-0.23	-0.2
Odd harmonics *DSIM*	25	-0.23	-0.2

Table 4: SAPF and Load Parameters

Per-phase Filter Inductance, L	2.5mH
DC link Filter Capacitor, C	4.7mF
Per-phase Line Inductance	1mH
Per-phase Line Resistance	0.01Ω
Rectifier Filter Inductance	500μH
Rectifier Filter Capacitance	4.7mF
Rectifier Load	30Ω

VII. SIMULATION RESULTS AND PERFORMANCE COMPARATIVE ANALYSIS

In this section are presented the simulation results of the steady-state and transient performance obtained with two of the cases presented in Tables 2 and 3. Even more, a performance comparative analysis between those cases is carried out. The simulation of the SAPF was performed in the power electronics and control software PSIM V9.04, using a three-phase three-leg converter with IGBT semiconductors. The control and compensation software was implemented in a DLL block which is an important tool that allows writing the source code in C language. This has the great advantage that the C code for the DLL block will be used almost entirely, within the DSC. Nonlinear load comprises: a three-phase diode rectifier with an LC filter and resistive load and their parameters are in Table 4.

In Fig. 7 is shown the steady-state response of the controlled system using the even and odd harmonics internal model based controller, that represent the worst case, while Fig. 8 shows the steady-state performance of the system with the odd harmonics *DSIM* based controller with $f_s = 0.5f_{sw}$, representing the best case. For the six cases presented in Tables 2 and 3, the steady-state performance in each case can be distinguished by the THD$_i$ values shown in Tables 5 and 6.

In Table 5, it is possible to appreciate that the best results (i.e., the lower THD$_i$) occur when using the *DSIM* strategy. Those results validate the claimed advantages of *DSIM* structures. In Table 6 the *DSIM* control strategies with f_s=0.5f_{sw} are shown. As can be seen,

Table 5. THD$_i$ of the line currents with $f_s = f_{sw}$

Internal Model Controllers	**THDi (%)**
Even and odd harmonics	9.22
Odd harmonics	9.19
Even and odd harmonics DSIM	3.04
Odd harmonics DSIM	2.24

Table 6. THD*i* of the line currents with $f_s = 0.5f_{sw}$

Internal Model Controllers	**THDi (%)**
Even and odd harmonics DSIM	2.83
Odd harmonics DSIM	2.83

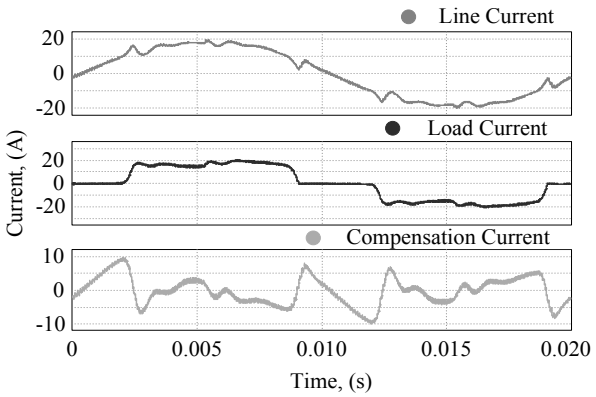

Figure 7: Simulation results. From top to bottom, line load and compensation currents. Even and odd harmonics internal model based controller.

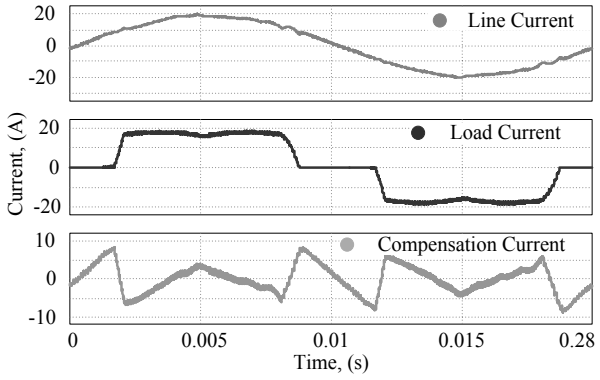

Figure 8: Simulation results. From top to bottom, line load and compensation currents. Odd harmonics *DSIM* based control.

the resulting THD$_i$ of the line currents are a little higher than the THD$_i$ values presented by *DSIM* control strategies in Table 5. Still, the values remain low. The increase in the THD$_i$ is explained by the reduced number of harmonics of this internal model controller.

Figure 9 presents the transient response of the inner current loop when the odd harmonics *DSIM* based controller with $f_s = 0.5f_{sw}$ is used. This case results with the lower settling time, and as seen, from the instant in which the active filter starts to operate; the current harmonic distortion is significantly reduced after one period of the fundamental frequency. This result again verifies the importance to reduce the sampling frequency of

the internal model based controller.

Finally, Fig. 10 shows the active and reactive power when the odd harmonics *DSIM* based controller with $f_s = f_{sw}$ is used. This controller configuration was selected because result in a lower current THD_i, in fact, this means lower reactive power on the grid side. As can be seen, the active power is almost constant and the reactive one is reduced significantly.

VIII. CONCLUSIONS

In this paper the analysis, design methodology and validation results for discrete-time controllers based on the internal model principle applied to SAPF are presented. These kinds of proposed controllers allow the suitable compensation of currents harmonics introduced by severe nonlinear loads currently present in low voltage grids. It has been observed that *DSIM* control strategies, in which the internal model based controller is sampled at lower frequencies than the classical compensator, offers much better results than the cases where both controllers are sampled at the same frequency. This downsampled internal model based controller, as claimed early, lets the reduction of the buffer size required for a digital implementation, significantly improving the transient response settling times and increase the stability margin of the closed-loop system. Although *DSIM* realization reduces the number of harmonics that can be compensated, the resulting current source THD_i remains below the limits established in the standards. The steady-state and transient performance of the proposed strategies was validated by simulation results and as expected the compensation of the active and reactive power for a balanced grid voltage condition and with several nonlinear loads has been accomplished by the SAPF.

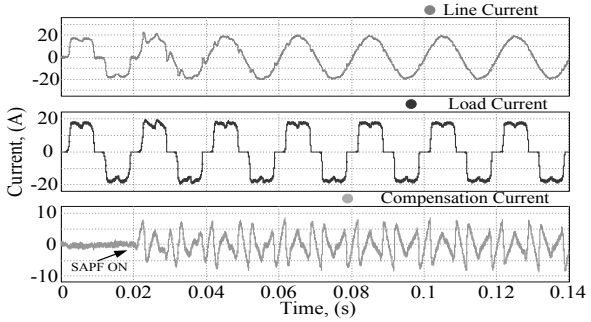

Figure 9: Transient response of the SAPF when used the odd harmonics *DSIM* based controller with $f_s = 0.5f_{sw}$.

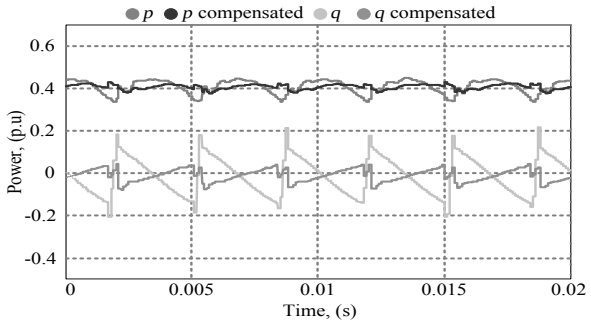

Figure 10: Active and reactive power with the odd harmonics *DSIM* based controller with $f_s = f_{sw}$.

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